CLAIMS

What is claimed is:

1. A magnetic memory comprising

a plurality of magnetic memory cells,

a plurality of magnetic write lines coupled with the plurality of magnetic memory cells, the plurality of magnetic write lines having a plurality of end regions; and

a plurality of magnetic biasing structures coupled to the plurality of end regions.

2. The magnetic memory of claim 1 wherein the plurality of magnetic biasing structures include a plurality of hard magnetic biasing structures coupled to the plurality of end regions.

3. The magnetic memory of claim 1 wherein the plurality of magnetic write lines include a plurality of tops and wherein the plurality of magnetic biasing structures include a plurality of antiferromagnetic biasing structures in contact with the plurality of tops and coupled to the plurality of end regions.

4. The magnetic memory of claim 1 wherein the plurality of magnetic write lines include a plurality of bottoms and wherein the plurality of magnetic biasing structures include a plurality of antiferromagnetic biasing structures in contact with the plurality of bottoms and coupled to the plurality of end regions.

5. The magnetic memory of claim 1 wherein the plurality of magnetic write lines include a plurality of tops and wherein the plurality of magnetic biasing structures are formed from the plurality of end regions, each of the plurality of biasing structures having a surface forming an angle with a top of the plurality of tops of a corresponding magnetic write line, the angle being different form a right angle.

6. The magnetic memory of claim 1 wherein the plurality of magnetic write lines include a plurality of magnetic bit lines electrically connected to the plurality or magnetic memory cells.

7. The magnetic memory of claim 6 wherein the plurality of magnetic memory cells include a plurality of magnetic tunneling junction stacks, each of the plurality of magnetic tunneling junction stacks includes a free layer, an insulator layer and a pinned layer, the free layer and the pinned layer being ferromagnetic, the insulator layer residing between the free layer and a pinned layer and having a thickness that allows tunneling of charge carriers between the free layer and the pinned layer.

8. The magnetic memory of claim 7 wherein the plurality of magnetic bit lines are separated from the free layer by less than or equal to three hundred Angstroms.

9. The magnetic memory of claim 8 wherein each of the plurality of magnetic

tunneling junction stacks includes a nonmagnetic spacer layer between the free layer and a corresponding magnetic bit line, the nonmagnetic spacer layer being conductive.

10. A method for utilizing a magnetic memory comprising the steps of:

(a) in a write mode, writing to a first portion of a plurality of memory cells, the plurality of memory cells being coupled to a plurality of magnetic write lines, the plurality of magnetic write lines having a plurality of end regions and carrying a current for writing to at least one of the plurality of magnetic memory cells, a plurality of magnetic biasing structures coupled to the plurality of end regions;

(b) in a read mode, reading from a second portion of the plurality of memory cells.

11. A method for providing a magnetic memory comprising

(a) providing a plurality of magnetic memory cells,

(b) providing a plurality of magnetic write lines coupled with the plurality of magnetic memory cells, the plurality of magnetic write lines having a plurality of end regions; and

(c) providing a plurality of magnetic biasing structures coupled to the plurality of end regions.

12. The method of claim 11 wherein the magnetic biasing structures providing

step (c) further includes the steps of:

(c1) providing a plurality of hard magnetic biasing structures coupled to the plurality of end regions.

13. The method of claim 11 wherein the plurality of magnetic write lines include a plurality of tops and wherein magnetic biasing structures providing step (c) further includes the steps of:

(c1) providing a plurality of antiferromagnetic biasing structures in contact with the plurality of tops and coupled to the plurality of end regions.

14. The method of claim 11 wherein the plurality of magnetic write lines include a plurality of bottoms and wherein the magnetic biasing structures providing step (c) further includes the steps of:

(c1) providing a plurality of antiferromagnetic biasing structures in contact with the plurality of bottoms and coupled to the plurality of end regions.

15. The method of claim 11 wherein the plurality of magnetic write lines include a plurality of tops and wherein the magnetic biasing structures providing step (c) further includes the step of:

(c1) forming the plurality of magnetic biasing structures from the plurality of end regions, each of the plurality of biasing structures having a surface forming an angle with a

top of the plurality of tops of a corresponding magnetic write line, the angle being different form a right angle.

16. The method of claim 11 wherein the magnetic write line providing step (b) further includes the step of:

(b1) providing a plurality of magnetic bit lines electrically connected to the plurality or magnetic memory cells.

17. The method of claim 16 wherein the magnetic memory cells providing step (a) further includes the steps of:

(a1) providing a plurality of magnetic tunneling junction stacks, each of the plurality of magnetic tunneling junction stacks includes a free layer, an insulator layer and a pinned layer, the free layer and the pinned layer being ferromagnetic, the insulator layer residing between the free layer and a pinned layer and having a thickness that allows tunneling of charge carriers between the free layer and the pinned layer.

18. The method of claim 17 wherein the plurality of magnetic bit lines are separated from the free layer by less than or equal to three hundred Angstroms.

19. The method of claim 18 wherein each of the plurality of magnetic tunneling junction stacks includes a nonmagnetic spacer layer between the free layer and a

corresponding magnetic bit line, the nonmagnetic spacer layer being conductive.